FAIRCHILD
SEMICONDUCTOR®

2N6897

-12A, -100V, P-Channel Enhancement Mode Power MOS Field Effect Transistor

December 2001

Features

- **-12A, -100V**
- **$r_{DS(ON)}$ = 0.3Ω**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Majority Carrier Device**

Description

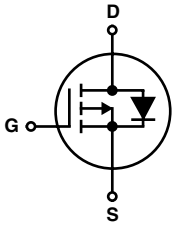
The 2N6897 is an P-Channel enhancement mode silicon gate power MOS field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This device can be operated directly from an integrated circuit.

Ordering Information

PART NUMBER	PACKAGE	BRAND
2N6897	TO-204AA	2N6897

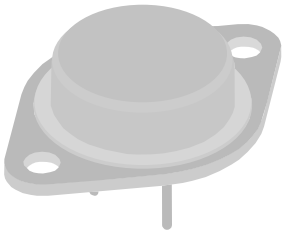
NOTE: When ordering, include the entire part number.

Symbol



Packaging

JEDEC TO-204AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		2N6897	UNITS
Drian to Source Voltage	BV_{DSS}	-100	V
Drian to Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	-100	V
Continuous Drain Current			
RMS Continuous	I_D	-12	A
Pulsed Drain Current	I_{DM}	-30	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
$T_C = 25^oC$	P_D	100	W
Above $T_C = 25^oC$, Derate Linearly		0.8	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Lead Temperature for Soldering (At distance 1/8 in. (3.17mm) from seating plane for 10s max)	T_L	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drian to Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V	-100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA	-2	-	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80V	-	-	1	µA
Zero-Gate Voltage Drain Current $T_C = 125^oC$		V_{DS} = -80V	-	-	50	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	100	nA
Drian to Source On-Voltage (Note 1)	$V_{DS(ON)}$	I_D = 7.6A, V_{GS} = -10V	-	-	2.28	V
		I_D =12A, V_{GS} = -10V	-	-	-4.8	V
Static Drian to Source On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 7.6A, V_{GS} = -10V	-	-	0.3	Ω
Static Drian to Source On Resistance $T_C = 125^oC$ (Note 1)		I_D = 7.6A, V_{GS} = 10V	-	-	0.465	Ω
Forward Transconductance (Note 1)	g_{fs}	I_D = 7.6A, V_{DS} = -10V	2	-	8	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V f = 0.1MHz	400	-	1500	pF
Output Capacitance	C_{OSS}		200	-	700	pF
Reverse-Transfer Capacitance	C_{RSS}		60	-	240	pF
Turn-On Delay Time	$t_{d(ON)}$	I_D = 7.6A, V_{DS} = -50V $R_{GEN} = R_{GS} = 15\Omega$, V_{GS} = -10V	-	-	60	ns
Rise Time	t_r		-	-	175	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	275	ns
Fall Time	t_f		-	-	175	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	-	1.25	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage (Note 1)	V_{SD}	I_{SD} = 12A	0.8	-	1.6	V
Diode Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/dt = 100A/µs	-	-	500	ns

NOTE:

4. Pulsed: pulse duration = 300µs, max, duty cycle = 2%.

Typical Performance Curves Unless Otherwise Specified

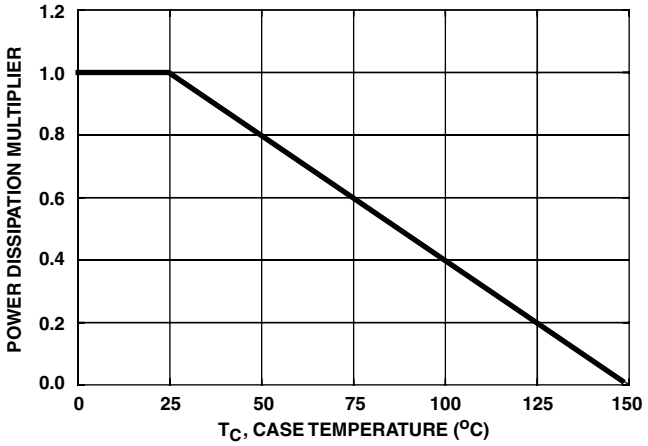


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

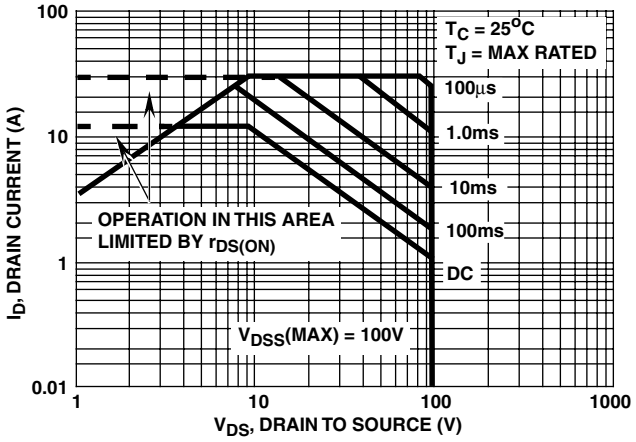


FIGURE 16. MAXIMUM OPERATING AREAS CURVE

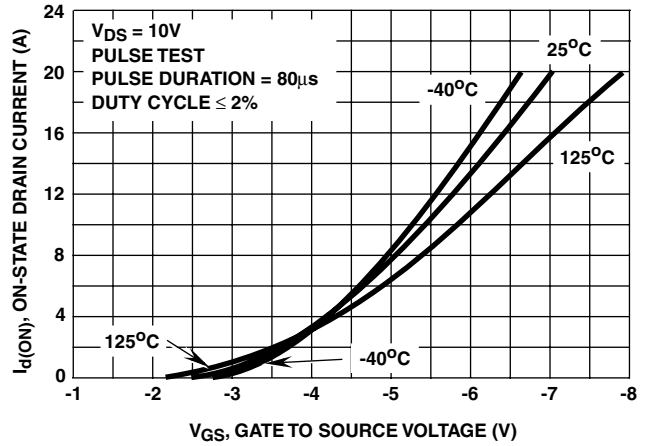


FIGURE 17. TRANSFER CHARACTERISTICS

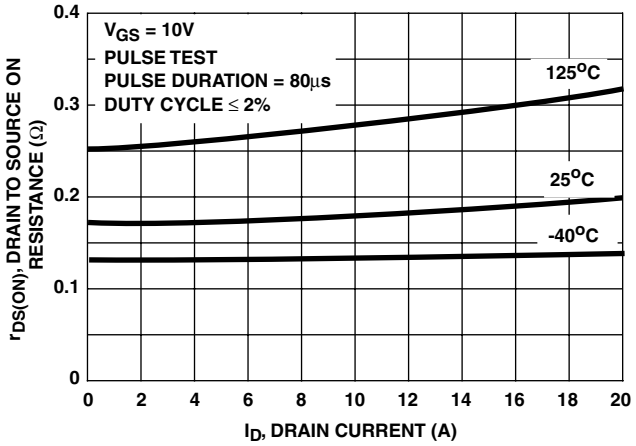


FIGURE 18. DRAIN TO SOURCE ON RESISTANCE AS A FUNCTION OF DRAIN CURRENT

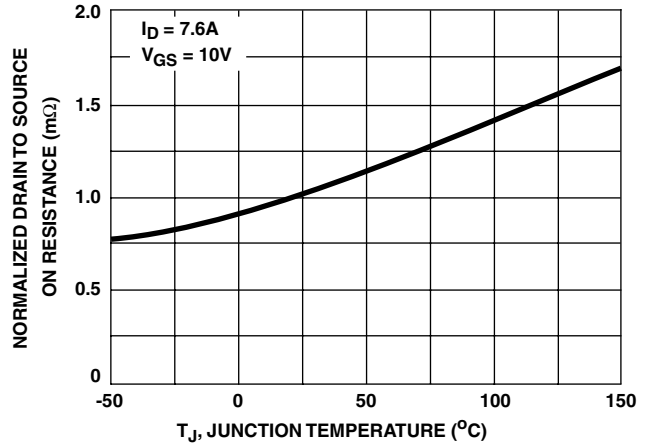


FIGURE 19. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

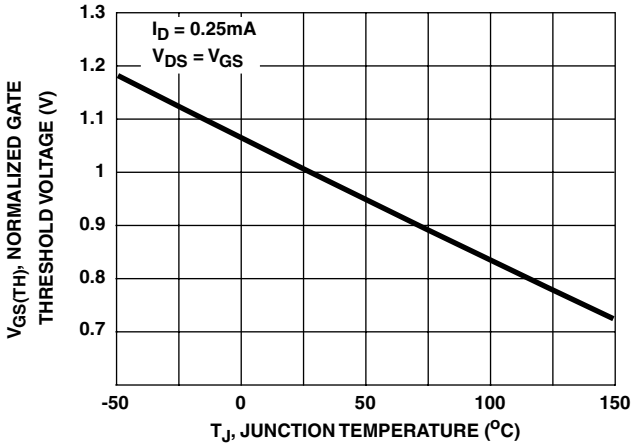


FIGURE 20. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

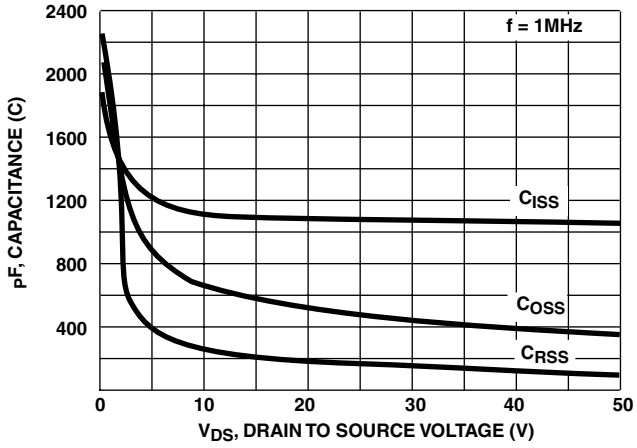


FIGURE 21. CAPACITANCE vs VOLTAGE

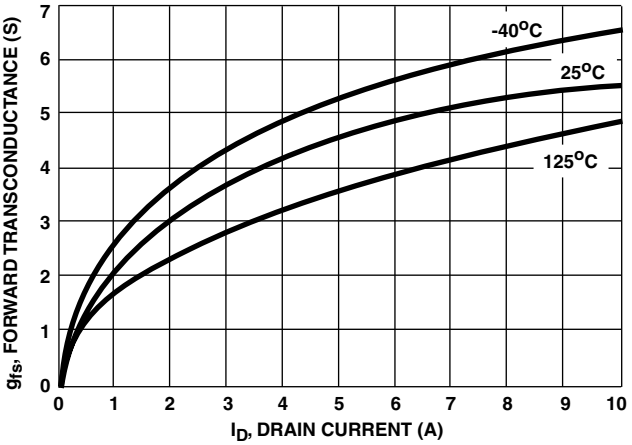


FIGURE 22. FORWARD TRANSCONDUCTANCE AS A FUNCTION OF DRAIN CURRENT

Test Circuit and Waveforms

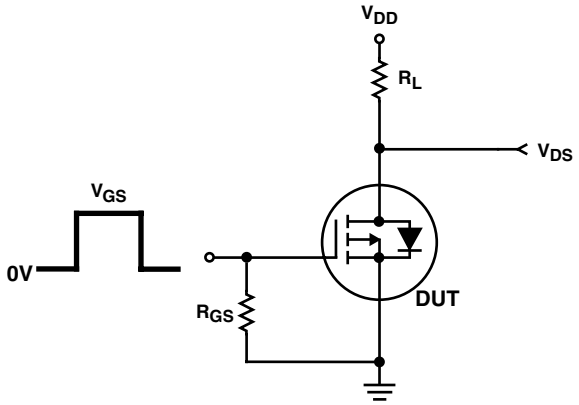


FIGURE 23. RESISTIVE SWITCHING TEST CIRCUIT

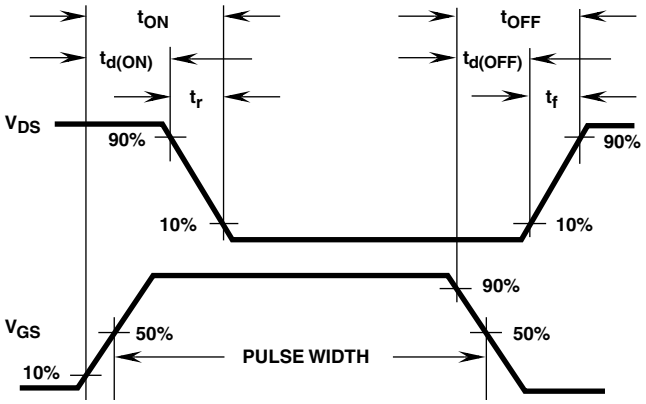


FIGURE 24. RESISTIVE SWITCHING WAVEFORMS

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DenseTrench™	GTO™	Power247™	SuperSOT™-6	
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